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(71) Applicant: FUJITSU LIMITED
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211 (JP)

(72) Inventor: Kiriseko, Tadashi
3-6-16, Wakabadai Shiroyama-cho
Tsukui-gun Kanagawa 220-01 (JP)

Tani, Hiromichi
109, 2-79-18, Furuichiba Saiwai-ku
Kawasaki-shi Kanagawa 211 (JP)

Soma, Noriko
1-6-5-405, Utsukushigaoka Midori-ku
Yokohama-shi Kanagawa 277 (JP)

Shigemi, Nobuhisa
Rm. 307, Dai-8 Nakahara-ryo, 1674, Shimokodanaka
Nakahara-ku Kawasaki-shi Kanagawa 211 (JP)

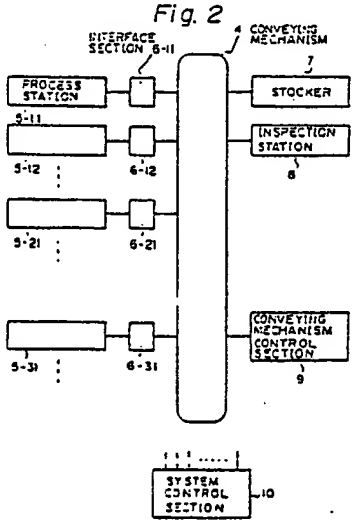
Toyoda, Takayuki
28, Uchihori-cho Yokkaichi-shi
Mie 510 (JP)

(74) Representative: Stebbing, Timothy Charles et al
Haseltine Lake & Co. Hazlitt House 28 Southampton
Buildings Chancery Lane
London WC2A 1AT (GB)

(54) Continuous semiconductor substrate processing system.

(57) A continuous semiconductor substrate processing system comprising a plurality of different process stations (5-11,5-12,...) for performing respective predetermined processes on semiconductor wafers and a semiconductor wafer conveying mechanism (4) coupled to the individual semiconductor wafer process stations. Each process station is coupled to the conveying mechanism via an interface section (6-11,6-12,...) including a transfer mechanism (11) for transferring semiconductor wafers between the conveying mechanism (4) and each process station (5-11,5-12,...), a discrimination section (13) for discriminating the semiconductor wafers, and a buffer section (12) for temporarily storing the semiconductor wafers. The continuous semiconductor wafer processing system further comprises: a stocker (7) coupled to the conveying mechanism (4) for temporarily accommodating semiconductor wafers during processing and including a storage section (15) for storing semiconductor wafers, a transfer mechanism (14) for transferring semiconductor wafers between said storage section and said conveying mechanism (4), a discrimination section (16) for discriminating semiconductor wafers, and a carrier feed-in feed-out section (17) capable of feeding in and feeding out semiconductor wafers; a conveying mechanism; and a system control section (10) for communicating with and controlling the process stations (5-11,5-12,...), interface sections (6-11,6-12,...), stocker (7) and conveying mechanism control section (9).

Fig. 2



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Description

CONTINUOUS SEMICONDUCTOR SUBSTRATE PROCESSING SYSTEM

This invention relates to a system for producing semiconductor devices and, more particularly, to a system for successively and continuously processing semiconductor substrates (wafers).

Usually, semiconductor devices are produced continuously and consistently by coupling individual process stations or units, which perform respective predetermined processes on semiconductor wafers, to one another by a conveying mechanism for conveying the semiconductor wafers.

In the prior art system, however, the entire processing system for producing semiconductor devices must be stopped when a fault occurs in any of the process stations or units or a part of the conveying mechanism, and if the recovery of the system requires a long time, a great reduction of the productivity and disarrangement of the production schedule occurs.

Therefore, the processing system should be capable of operating even when a part thereof is under maintenance due to a fault occurrence.

(1) Processing System for Producing Semiconductor Devices

In the production of a large quantity of few fa'uds products such as DRAM's (dynamic random access memories), a plurality of production process items cannot be carried out at one time in the same semiconductor wafer processing system, and therefore, semiconductor devices can be produced only by processing semiconductor wafers in a proper order and by a fixed procedure.

On the other hand, in the production of a small quantity of many kinds of products such as ASIC (application specific integrated circuits), a plurality of process items must be carried out simultaneously in a semiconductor wafer processing system to meet a given term (delivery date).

Currently, a continuous semiconductor wafer processing system having a wide freedom of choice of many process items is required, to meet the demand for a small quantity of many kinds of semiconductor device products, including ASIC.

(2) Example of Prior Art Continuous Processing System

A prior art continuous processing system is disclosed in Japanese Patent Publication 59-31211, corresponding to USP 3946484, and Fig. 1 is a schematic plan view of this disclosed system.

The system comprises independent wafer-processing stations or units 1A to 1F and a central conveying unit 2 for transferring wafers to and from the individual stations or units by a reciprocal operation. A continuous processing of wafers is made possible by coupling the individual process stations or units with the central conveying unit 2.

As an example, a processing procedure for manufacturing FET (field effect transistor) will now be described.

(1) Wafers are supplied from a Loader 3 to an initial oxidization station 1A.

(2) Cleaning of the wafer surface, formation of an initial oxide film, and coating of a photoresist are carried out in the initial oxidization station 1A.

(3) The central conveying unit 2 picks up wafers after the process (2) and conveys them to a photoresist exposure station 1D.

(4) Exposure to predetermined pattern is made in the photoresist exposure station 1D.

(5) The central conveying unit 2 picks up wafers after the process (4) and conveys them to a drain station 1B.

(6) Development of the photoresist, etching of the oxide film, and formation of a drain region by diffusion are carried out in the drain station 1B.

The photoresist is then coated.

(7) The central conveying station 2 picks up wafers after the process (6) and conveys them again to the photoresist exposure station 1D.

(8) A gate region pattern exposure is carried out in the photoresist exposure station 1D.

(9) The central conveying unit 2 picks up wafers after the process (8) and conveys them to a gate station 1C.

(10) Development of the photoresist, etching and the formation of an oxide film are carried out in the gate station 1C.

The photoresist is again coated.

(11) The central conveying unit 2 picks up wafers after the process (10) and conveys them to the photoresist exposure station 1D again.

(12) Exposure to a predetermined pattern is carried out in the photoresist exposure station 1D.

(13) The central conveying unit 2 picks up wafers after process (12) and conveys them to a metallization station 1E.

(14) Development of the photoresist, etching, and a metallization of the wafer surface are carried out in the metallization station 1E.

The photoresist is again coated.

(15) The central conveying unit 2 picks up wafers after the process (14) and conveys them to the photoresist exposure station 1D again.

(16) Exposure to a predetermined pattern is made in the photoresist exposure station 1D.

(17) The central conveying unit 2 picks up wafers after the process (16) and conveys them to a sintering station 1F.

Development of the photoresist, etching of the metallic film, and sintering of the wafer are carried out in the sintering station 1F.

Thereafter, the wafers are collected in an unloader 104, thus ending the processing of the wafers.

As shown above, a series of processes on the wafers is completed by conveying wafers to individual process stations for processing wafers in a predetermined sequence.

In the above processing system, however, once a

fault occurs in any of the process stations 1A to 1F or in a part of the central conveying unit 2, the series of wafer processes can no longer be continued, that is, the entire processing system must be stopped, thus leading to an extreme reduction of the productivity and a disturbance of the production schedule.

In addition, the processing in this case gives priority to the processing of preceding wafers. This means that the speed of processing (or processing time of) a succeeding wafer is prescribed by the speed of processing a preceding wafer. In other words, the processing efficiency is determined by the processing time of a slowest process station operating at a lowest processing speed among the process stations.

Therefore, where a plurality of different kinds of products are produced, the throughput of the processing system is greatly reduced due to a difference in the processing times among various process items.

It is therefore desirable to solve the above problems inherent in the prior art continuous semiconductor wafer processing system, and to realize a processing system which is capable of operating even when a fault occurs in or during a maintenance of a part thereof, so that fewer processing efficiency variations occur even when producing a plurality of different kinds of products at one time, is given a wide freedom of choice of process items, and has a high productivity.

According to the present invention there is provided a continuous semiconductor wafer processing system comprising a plurality of different process stations for performing respective predetermined processes on semiconductor wafers and a semiconductor wafer conveying mechanism coupled to said individual semiconductor wafer process stations ;

each process station being coupled to said semiconductor wafer conveying mechanism via an interface section including a transfer mechanism for transferring semiconductor wafers between said conveying mechanism and each of said process stations , a discrimination section for discriminating said semiconductor wafers, and a buffer section for temporarily storing said semiconductor wafer;

said continuous semiconductor wafer processing system further comprising:

a stocker coupled to said conveying mechanism for temporarily accommodating semiconductor wafers during the processing and including a storage section for storing said semiconductor wafers, a transfer mechanism for transferring semiconductor wafers between said storage section and said conveying mechanism , a discrimination section for discriminating said semiconductor wafers, and a carrier feed-in feed-out section capable of feeding in and feeding out said semiconductor wafers; and

a conveying mechanism control section for controlling said conveying mechanism and a system control section for communicating with and controlling said process stations , interface sections , stocker and conveying mechanism control section.

Reference is made, by way of example, to the accompanying drawings in which:-

Figure 1 is a plan view for explaining a prior art processing system.

Figure 2 is a block diagram for explaining the principles underlying the invention;

Fig. 3 is a block diagram for explaining the basic construction of an interface section;

Fig. 4 is a block diagram for explaining the basic construction of a stocker;

Fig. 5A to 5D are a flow chart for explaining a first mode of system operation procedure;

Fig. 6A and 6B are a flow chart for explaining a second mode of system operation procedure;

Fig. 7 is a block diagram for explaining an embodiment;

Fig. 8 is a flow chart for explaining a processing of a wafer to manufacture an ASIC, with basic operation steps being shown in (a) and a subroutine between adjacent steps being shown in (b);

Fig. 9 is a block diagram showing an example of an interface section;

Fig. 10 is for explaining an actual construction of interface section, with (a) being a perspective view of the interface section and (b) being a perspective view of a carrier;

Fig. 11 is a block diagram for explaining an example of a stocker;

Fig. 12 is a plan view showing an actual construction of a stocker;

Fig. 13 is a block diagram for explaining a small scale conveying mechanism along process stations; and

Fig. 14 is a perspective view for explaining a way in which each process station is ~~coupled to~~ a conveying mechanism.

Before describing a preferred embodiment, the principle of the present invention will be explained.

Figure 2 is a block diagram for explaining the principles underlying the invention, Fig. 3 is a block diagram for explaining the basic construction of an interface section, and Fig. 4 is a block diagram for explaining the basic construction of a stocker.

The processing system according to the invention has the features that it can temporarily store wafers, it can set a priority order of the processing of wafers, and that it can convey wafers by a carrier.

(1) Basic Construction

A continuous semiconductor wafer processing system of the present invention comprises a plurality of different process sections 5 for performing respective predetermined processes on semiconductor wafers, and a semiconductor wafer conveying mechanism 4 coupled to the individual semiconductor wafer process stations 5; each process station 5 being coupled to the semiconductor wafer conveying mechanism 4 via an interface section 6 including a transfer mechanism 11 for transferring semiconductor wafers between the conveying mechanism 4 and each process station 5, a discrimination section 13 for discriminating the semiconductor wafers and a buffer section 12 for temporarily storing the semiconductor wafers.

The continuous semiconductor wafer processing

system further comprises: a stocker 7 coupled to the conveying mechanism 4 for temporarily accommodating semiconductor wafers during processing, and including a storage section 15 for storing the semiconductor wafers, a transfer mechanism 14 for transferring semiconductor wafers between the storage section 15, and a conveying mechanism 14, a discriminating section 16 for discriminating the semiconductor wafers, and a carrier feed-in feed-out section 17 capable of feeding in and feeding out the semiconductor wafers; and a conveying mechanism control section 9 for controlling the conveying mechanism 4 and a system control section 10 for communicating with and controlling the process stations 5, interface sections 6, stocker 7, and conveying mechanism control section 9.

Further, the system further comprises an inspection section 8 for inspecting semiconductor wafers processed in the individual process stations 5, and if necessary, a plurality of sections 5-11, 5-12, ... for performing the same process may be provided as the process section 5.

(2) Construction Permitting Semiconductor Wafers to be Conveyed by Carrier

In the construction (1) described above, the buffer section 12 of the interface section 6 includes a carrier capable of carrying semiconductor wafers and being mounted in and dismounted from the interface section 6 for conveying the semiconductor wafers, the carrier being capable of being mounted in the carrier feed-in feed out section 17 of the stocker 7.

A continuous semiconductor wafer processing system of the present invention has the following functions.

(1) One-by-one management of semiconductor wafers

1) The interface section 6 has a discrimination section 13 for discriminating individual semiconductor wafers for a one-by-one management of wafers transferred from the conveying mechanism 4 to the process section 5.

2) The stocker 7 has a discrimination section 16 capable of discriminating individual wafers for a one-by-one management of semiconductor wafers transferred from the conveying mechanism 4 to a storage section 15.

3) The conveying mechanism control section 9 controls the conveying mechanism 4 according to instructions from the system control section 10, to convey wafers one by one to given process stations.

4) The system control section 10 makes decisions on the contents of processing of wafers and control of conveying and progress of processing of wafers by communicating with and controlling the process stations 5, interface sections 6, stocker 7, and conveying mechanism control section 9.

More specifically, the continuous semiconductor wafer processing system of the present invention can process individual wafers one by one in accordance with process contents, processing procedures, and processing schedules programmed in the system control section 10.

(2) Flexibility of Process Priority Order among Semiconductor Wafers

The buffer section 12 of the interface section 6 temporarily stores semiconductor wafers conveyed thereto by the conveying mechanism 4, and the transfer mechanism 11 transfers wafers to the process station 5 according to a process procedure given by the system control section 10.

More specifically, the continuous semiconductor wafer processing system of the present invention can determine the priority order of the processing of wafers not on the basis of the order in which wafers are conveyed to the interface section 6, but on the basis of a processing schedule provided by the system control section 10.

(3) Flexibility of Process Balance among Individual Process Stations

If there is a deviation from the timing of processing on each semiconductor substrate in each process station 5, the processes in the individual process stations 5 become unbalanced, so that a redundancy availability reception of wafers for the next process will be lost.

In such a case, the system control section 10 temporarily stores predetermined wafers to be conveyed to the next process station in the stocker 7 and instructs the conveying mechanism 4 and stocker 7 to convey the wafers to the next process station when the next process station becomes ready to receive the wafers.

This means that the continuous semiconductor wafer processing system of the present invention has a flexible redundancy ensuring smooth continuous processing even when there a delay occurs in the processing by the individual process stations 5 operating in an non-synchronous fashion.

(4) Flexibility with Respect to Faults in and Maintenance of Conveying Mechanism

A carrier for conveying wafers can be mounted in the buffer section 12 of the interface section 6, and in the carrier feed-in/out section 17 of the stocker 7.

This means that it is possible to convey wafers without the conveying mechanism 4.

The preferred embodiment will now be described.

(1) System Operation Procedure

A description will now be given of how a series of process operations is actually performed in the continuous semiconductor wafer processing system having the basic construction as described before with reference to Figs. 2 to 4.

The above continuous semiconductor wafer processing system is capable of setting a first mode of system operation procedure in which wafers are conveyed by the conveying mechanism, and a second mode of system operation procedure in which wafers are conveyed without using the conveying mechanism.

1) First Mode of System Operation Procedure

Figure 5A to 5B are flow charts for explaining the first mode of system operation procedure. In this case, operations are performed in the order of the charts of Figs. 5A to 5D.

The procedure will now be described sequentially.

(1) When receiving a certain lot for processing by a given process station 5, wafers are discriminated one by one by the discrimination section 13 of the associated interface section 6, to be stored in the buffer section 12 thereof.

(2) The interface section 6 transmits the wafer discrimination results to the system control section 10, and the system control section 10 determines the priority order of the processing of the wafers in the buffer section 12 and sends an instruction to start the processing.

(3) The process station 5 processes the wafers as instructed by the system control section 10.

(4) When checking whether the process (3) is correct, the system control section 10 sends an instruction to the conveying mechanism control section 9 to allow each wafer be conveyed to the inspection section 8.

(5) The inspection section 8 carries out a wafer inspection as instructed by the system control section 10 and if necessary, measures the physical and electrical status of the process.

(6) When the inspection (4) is unnecessary or when the inspection and measurement in (5) are finished, the system control section 10 instructs the conveying mechanism control section 9 to allow the wafers to be conveyed to the next process station. When sending this conveying instruction, the system control section 10 checks the operating status of the next process station 5, and if it is detected that the operation is suspended or if the amount of work supplied is excessive, instructs the conveying mechanism control section 9 to allow the wafers to be conveyed to the stocker 7.

(7) The wafers conveyed to the stocker 7 in (6) are discriminated in the discrimination section 16 and then stored in the storage section 15.

(8) When detecting that the next process station 5 is in operating duty service and that the amount of work supplied is adequate, the system control section 10 instructs the stocker 7 to allow wafers stored in the stocker (7) to be taken out, discriminated in the discrimination section 16, and transferred to the conveying mechanism 4.

Then, the section 10 instructs the conveying mechanism control section 9 to allow the wafers to be conveyed to the next process.

(9) When the same number of process stations are provided for the next process to which the wafers are conveyed in (6) and (8), the system control section 10 compares the amount of work in the plurality of process stations and allows wafers to be conveyed to a station or stations to which it is determined that wafers can be conveyed.

(10) The next process station 5 receives wafers of the next lot.

Then, the routine returns to the start of the processing to repeat the same sequence of operations until a given processing of wafers is completed.

2) Second Mode of Operation Procedure

Figure 6A and 6B are flow charts for explaining the second mode of system operation procedure. In this case, operations are performed in the order of the charts of Figs. 6A and 6B.

The procedure will now be described sequentially.

(1) A carrier carrying a certain lot of wafers is mounted in the buffer section 12 of an interface section 6 pertaining to a given process station 5.

(2) The interface section 6 discriminates the wafers in the carrier one by one in the discrimination section 13 and then stores them in the buffer section 12.

Then, the section 6 transmits the wafer discrimination results to the system control section 10, and the system control section 10 determines the priority order of the processing of the wafers in the buffer section 12, and sends an instruction to start the processing.

(3) The process station 5 in (1) processes the wafers as instructed by the system control section 10, and when the processing is completed, stores the wafers in the buffer section 12.

(4) After the processing in (3) of all of the wafers is completed, the carrier is conveyed to the stocker 7 and mounted in the carrier feed-in feed-out section 17 by for example the operator.

(5) The stocker 7 discriminates the wafers in the carrier in the discrimination section 16, and then stores the wafers in the storage section 15 while transmitting the wafer discrimination results to the system control section 10.

(6) The system control section 10 instructs the stocker 7 to allow only wafers to be processed in the same process station for the next process to be transferred to the carrier.

(7) The stocker 7 takes out wafers from the storage section 15 for discrimination in the discrimination section 16, and allows only wafers to be processed in the same process station for the next process to be transferred to the carrier in the carrier feed-in/out section 17.

(8) The carrier in (7) is conveyed to the process station 5 as instructed by the system control section 10 by for example, the operator.

Then, the routine returns to start of the processing to repeat the same sequence of operations until a given processing of the wafers is completed.

It is possible to allow the carrier to be conveyed by a robot instead of the operator. Further, the system control section 10 may instruct the operator to convey the carrier to the next process, through a display on display means provided on the stocker 7 or interface section 6.

(2) Overall Construction of Continuous Semiconductor Wafer Processing System

Figure 7 is a block diagram for explaining an embodiment of the invention applied to a continuous semiconductor wafer processing system for producing an ASIC with a gate array.

This system comprises two electron beam exposure stations, two stepper exposure stations, one

photoresist coating station, one photoresist development station, two aluminum etching stations, two PSG (phosphosilicate glass) etching stations, two aluminum deposition stations, two PSG depositing stations, three inspection stations, two stockers, one measuring unit, and one numbering unit. The individual stations and units except for the stockers are coupled to a conveying mechanism via respective interface sections 18-6 to 34-6, 37-6 and 38-6.

A system control section 10a on-line communicates with and controls the individual components (i.e., stations, units, interface sections and stockers), and contains data of the contents of the processing of individual wafers to be processed and is aware of the status of the progress of the processing.

In the above construction, it is particularly important that the process stations need not consist of a plurality of stations. For example, only a single station may be provided for a process, in which only a short time is necessary for a recovery from a fault, while a plurality of process stations may be provided for a process in which long time is required for a recovery from a fault, such as a process performed in vacuum.

This is because, in the event of a fault in one of a plurality of process stations provided for the same process, the other stations can still carry out the processing, and thus it is possible to avoid a long-time suspension of the processing.

(3) Example of Processing of Wafers

An ASIC with a gate array is manufactured by providing a predetermined wiring to a bulk wafer with a matrix array of basic logic elements.

In this case, the wiring is provided using aluminum, and insulation between adjacent aluminum wiring layers is provided by using PSG.

Figure 8 is a flow chart for explaining the processing of wafers when manufacturing the ASIC, wherein (a) is a flow chart for explaining the overall sequence of basic operation steps, and (b) is a subroutine provided between adjacent steps.

The subroutine is provided to temporarily store wafers in the stocker when the next process station is busy.

(1) Step 1
Bulk wafers (semiconductor wafers) after aluminum is deposited are stored in the first stocker 35.

(2) Step 2
The bulk wafers are conveyed to the numbering unit 38, and wafer numbers are given in the form of bar codes to the bulk wafers to compile a manufacturing lot.

(3) Step 3
A photoresist is coated at the photoresist coating station 22.

(4) Step 4
A first aluminum wiring layer is exposed at the first or second electron beam exposure station 18 or 19.

(5) The photoresist is developed at the photoresist development station 23.

(6) Step 6
The first aluminum wiring layer is etched at the first or second aluminum etching station 24 or 25.

(7) Step 7
An inter-layer insulation film is formed at the first or second PSG deposition station 30 or 31.

(8) Step 8
Photoresist again coated at the photoresist coating section 22.

(9) Step 9
The second aluminum wiring layer is exposed at the first or second stepper exposure station 20 or 21, to form contact windows.

(10) Step 10
The photoresist is developed at the photoresist development station 23.

(11) Step 11
PSG layer is etched at the first or second PSG etching station 26 or 27.

(12) Step 12
An aluminum layer as a next wiring layer is formed at the first or second aluminum depositing station 28 or 29.

Subsequently, the routine returns to step 3, and accordingly, the second and third layer wirings are formed to complete the prescribed logic ASIC wafers.

In the individual steps, a process station having an adequate amount of work supplied thereto is selected, and the priority order of the processing in the individual process stations is determined by a production schedule programmed in the system control section 10a.

The same procedure is followed when wafers are conveyed without using the conveying mechanism 4a (for example, conveyed by an operator or a robot) except that the first or second stocker 33 or 36 is used when conveying the carrier carrying wafers.

(4) Interface Section

Figure 9 is a block diagram showing an example of the interface section.

In this example, interface sections 6a and 6b are provided on the respective inlet and outlet sides of each process station 5a. The individual interface sections 6a and 6b respectively include buffers 12a and 12b, discrimination sections 13a and 13b, and transfer mechanisms 11a and 11b, and further include respective control sections 39a and 39b for a control of the operation thereof.

The process station 5a includes a control section 40 for controlling the processing thereby.

A step control section 41 collectively controls the control sections 39a and 39b to provide a working synchronization of the interface sections 6a and 6b and process station 5a.

The control sections 39a, 39b, 40 and 41 communicate with and are controlled by the system control section 10a shown in Fig. 6.

Figure 10 shows an actual construction of the interface section, wherein (a) is a perspective view of the interface section, and (b) is a perspective view of a carrier.

This example of an interface section includes a handler 11c for transferring wafers 42, a bar code

reader 13c for discriminating the wafers 42, and a carrier 43 as buffer section 12c for temporarily storing the wafers 42. An elevator 43 is provided for conveying the wafers 42 vertically where the conveying mechanism and interface section have different installation heights.

The carrier 43 can be mounted in and dismounted from the buffer 12c, and has a grip 46 so that it can be readily conveyed by an operator.

(5) Stocker

Figure 11 is a block diagram showing an example of a stocker.

This example of the stocker 7a has independent carrier feed-in and feed-out sections 17a and 17b, and includes a storage section 15a, a discrimination section 16a, and a transfer mechanism 14a, and further, a control section 47 for controlling the operation thereof.

The control section 47 communicates with and is controlled by the system control section 10a shown in Fig. 6.

Figure 12 is a plan view showing an actual construction of a stocker.

This example of a stocker includes a handler 14d for transferring wafers 42, a storage section 15a for storing wafers, a bar code reader 16b for discriminating wafers, a carrier inlet 48 for feeding a carrier 45 therein, a carrier outlet 49 for feeding the carrier 45 therefrom, a handler 14c for taking out wafers 42 from the carrier 45, and a handler 14b for storing wafers in the carrier 45.

The bar code reader 16b is provided at a position past that at which wafers 42 can be moved from the conveying mechanism 4a and from the carrier 45, so that bar codes can be read out from wafers 42 transferred with by the conveying mechanism 4a and those transferred by the carrier 45.

(6) Small-scale conveying Mechanism

Figure 13 is a block diagram for explaining a small-scale conveying mechanism together with process stations.

Often the space utilization factor of a plant is lowered when all of the process stations are coupled to a conveying mechanism.

In such a case, it is better to provide the conveying mechanism 4a with a small-scale conveying mechanism 4b, to which the process stations 5a to 5d are coupled.

It is necessary, however, to provide a wafer transfer mechanism 50 between the conveying mechanism 4a and small-scale conveying mechanism 4b.

Figure 14 is a perspective view showing a way in which a process station is coupled to the conveying mechanism.

A small-scale conveying mechanism 4b extends above individual process stations 5a to 5d, and interface sections 6a and 6b and an elevator 43 are provided for the transfer of wafers between each of the process stations 5a to 5d and the small-scale conveying mechanism 4b.

Wafers are then conveyed to process station 51.

The continuous semiconductor wafer processing system as described above embodying the invention has the following features.

(1) One-by-one management of semiconductor wafers is possible.

(2) An interface section is provided between each process station and the conveying mechanism, and the interface section can set the priority order of the temporary storage of wafers and processing of the stored wafers.

(3) When a next process station to which wafers are to be conveyed is not operative or is holding an excessive quantity of work, wafers to be supplied are temporarily stored in a stocker until the start of a resumption of processing or until the quantity of work held in the process station is reduced to an extent such that it can receive wafers.

(4) Where a plurality of identical process stations are provided for the next process to which wafers are to be conveyed, wafers are conveyed to one of these stations holding the least quantity of work.

(5) On-line control by the system control section is possible even when a fault occurs in or during maintenance of the conveying mechanism, and it is possible to permit operation of the processing system by conveying wafers not with the conveying mechanism but on a carrier-by-carrier basis.

The continuous semiconductor wafer processing system according to the invention thus has the following effects.

(1) The operation of the processing system is possible even when a fault occurs or during maintenance of the conveying mechanism, so that it is possible to minimize delay of the production schedule.

(2) It is possible to give priority to a processing of wafers which will otherwise cause delay in the production schedule. Thus, it is possible to meet a delivery term of a plurality of lots of semiconductor wafers simultaneously, at a high level.

(3) A plurality of different kinds of wafers can be processed concurrently, and their delivery terms can be met simultaneously and at a high level even if their processing timings are different.

As shown above, it is possible to realize a continuous semiconductor wafer processing system which is very flexible with respect to a continuous processing of a plurality of different lots or different kinds of wafers, and has a high productivity.

Claims

1. A continuous semiconductor substrate processing system comprising a plurality of different process stations (5) for performing respective predetermined processes on semiconductor wafers and a semiconductor wafer conveying mechanism (4) coupled to said individual semiconductor wafer process sta-

tions (5);
each process station (5) being coupled to said semiconductor wafer conveying mechanism (4) via an interface section (6) including a transfer mechanism (11) for transferring semiconductor wafers between said conveying mechanism (4) and each of said process stations (5), a discrimination section (13) for discriminating said semiconductor wafers, and a buffer section (12) for temporarily storing said semiconductor wafers;
said continuous semiconductor wafer processing system further comprising:
a stocker (7) coupled to said conveying mechanism (4) for temporarily accommodating semiconductor wafers during the processing and including a storage section (15) for storing said semiconductor wafers, a transfer mechanism (14) for transferring semiconductor wafers between said storage section (15) and said conveying mechanism (14), a discrimination section (16) for discriminating said semiconductor wafers, and a carrier feed-in feed-out section (17) capable of feeding in and feeding out said semiconductor wafers; and
a conveying mechanism control section (9) for controlling said conveying mechanism (4) and a system control section (10) for communicating with and controlling said process stations (5), interface sections (6), stocker (7) and conveying mechanism control section (9).

2. A continuous semiconductor wafer processing system according to claim 1, which further comprises an inspection station (8) coupled to said conveying mechanism (4) for inspecting semiconductor wafers processed in each of said process stations (5).

3. A continuous semiconductor wafer processing system according to claim 1 or 2 wherein said buffer section (12) of said interface section (6) consists of a carrier capable of carrying semiconductor wafers and being mounted in and dismounted from said interface section (6) and for conveying said semiconductor wafers, said carrier able to be mounted in said carrier feed-in feed-out section (17) of said stocker 7.

4. A continuous semiconductor wafer processing system according to claim 1,2, or 3, wherein:
said conveying mechanism (4) conveys semiconductor wafers;
said system control section (10) communicates with and thereby controls said process stations (5), interface sections (6), stocker (7) and conveying mechanism control section (9) for conveying semiconductor wafers to each of said process stations (5) according to a procedure preliminarily programmed therein so that said wafers may be continuously processed;
said semiconductor wafers are conveyed to said stocker (7) if a next process station (5), to which said semiconductor wafers are to be conveyed, is holding work in excess of a permissible amount, said semiconductor wafers conveyed to said stocker (7) being discriminated in a discrimination section (16) and then stored in a storage section (15);
when said next process station becomes ready to receive semiconductor wafers, said semiconductor wafers in said storage section (16) of said stocker (7) being taken out sequentially according to a program of said system control section (10), to be discriminated in said discrimination section (16) and then conveyed to said next process station; and
the priority order of processing individual semiconductor wafers in each said process station (5) is determined by said system control section (10) through communication thereof with the associated interface section (6), said determination being carried out sequentially with respect to semiconductor wafers which have been discriminated in said discrimination section (13) of said interface section (6) and then stored in said buffer section (12) thereof according to a program of said system control section (10).

5. The continuous semiconductor wafer processing system according to claim 1, 2, 3 or 4 wherein a plurality of identical process stations (5-11, 5-12, ...) for performing the same process are provided as each of said process stations (5), and semiconductor wafers are conveyed to the next process station (5) by selecting one of said plurality of identical process stations (5-11, 5-12, ...), the buffer section (12) of the associated interface section (6) of which as the greatest prevailing capacity.

6. The continuous semiconductor wafer processing system according to claim 4 as appended to claim 3, wherein, when a fault occurs in or during maintenance of said conveying mechanism (4), semiconductor wafers are conveyed without said conveying mechanism (4);
said control section (10) communicating with and thereby controlling said process sections (5), interface sections (6) and stocker (7) to ensure that semiconductor wafers are conveyed on a carrier-by-carrier basis to said process stations (5) according to a predetermined program of said system control section (10) so that said semiconductor wafers are continuously processed, said carrier being mounted in said carrier feed-in/feed-out section (17) of said stocker (7) when conveying said carrier from a process station to a next station;
said semiconductor wafers in said carrier being individually discriminated in said discrimination section (16) of said stocker (7) and then temporarily stored in said storage section (15) thereof, only semiconductor wafers to be conveyed to said next process station being taken out from said storage section (15) according to an instruction from said system control section (10), to be individually discriminated in said discrimination section (16) and then accommodated in a carrier mounted in

said carrier feed-in/out section (17);
the carrier after completion of accommodation not being conveyed by said conveying mechanism (4) to said next process station;
the priority order of processing of individual semiconductor wafers in each of said process stations (5) being determined by said system control section (10) through communication thereof with the associated interface section (6), said determination being carried out sequentially with respect to semiconductor wafers, which have been determined in said discrimination section (13) of said interface section (6) and then stored in said buffer section (12) thereof, according to a program of said system control section (10).

Fig. 1

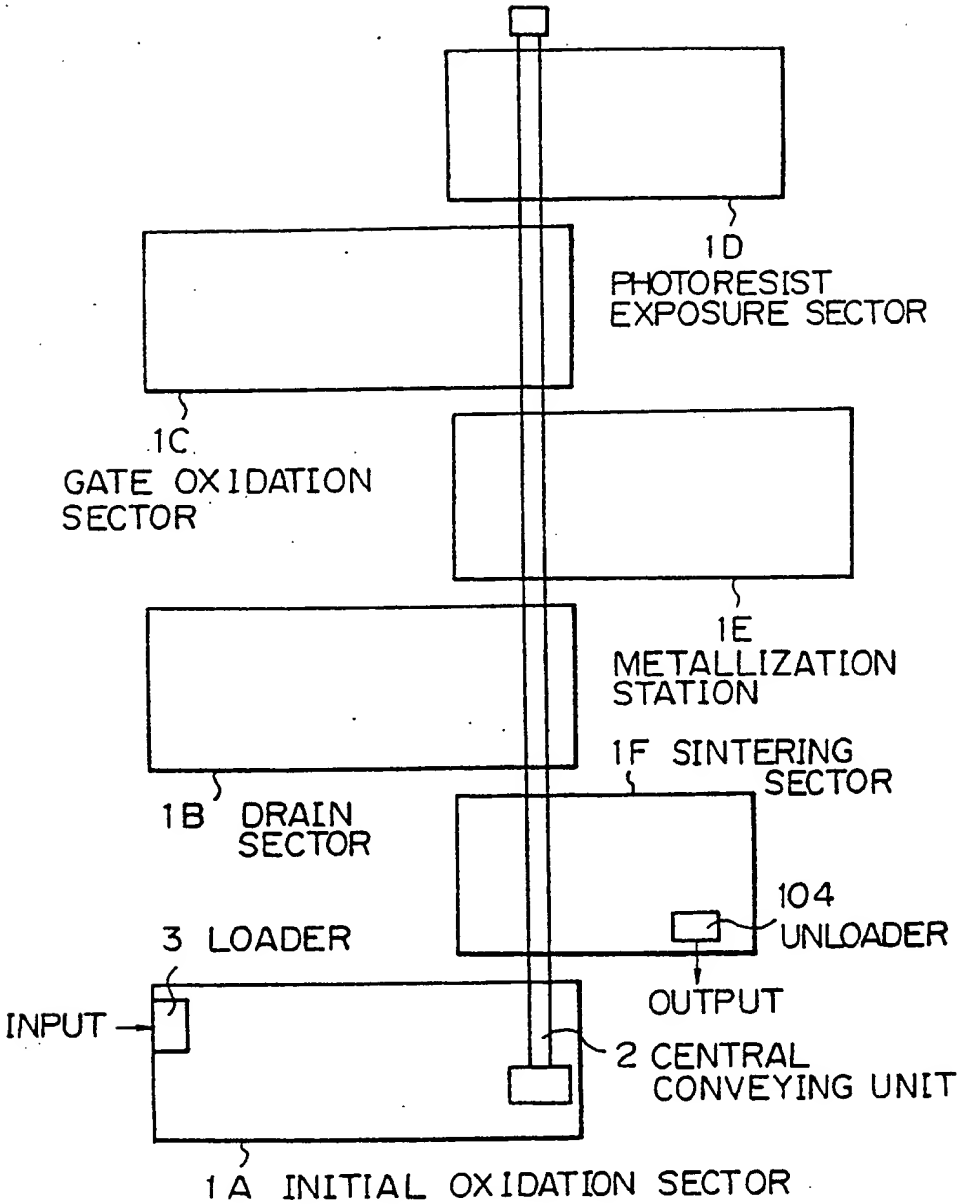

1D
PHOTORESIST
EXPOSURE SECTOR
1C
GATE OXIDATION
SECTOR
1E
METALLIZATION
STATION
1F SINTERING
SECTOR
1B DRAIN
SECTOR
104
UNLOADER
3 LOADER
OUTPUT
INPUT
2 CENTRAL
CONVEYING UNIT
1A INITIAL OXIDATION SECTOR

Fig. 2

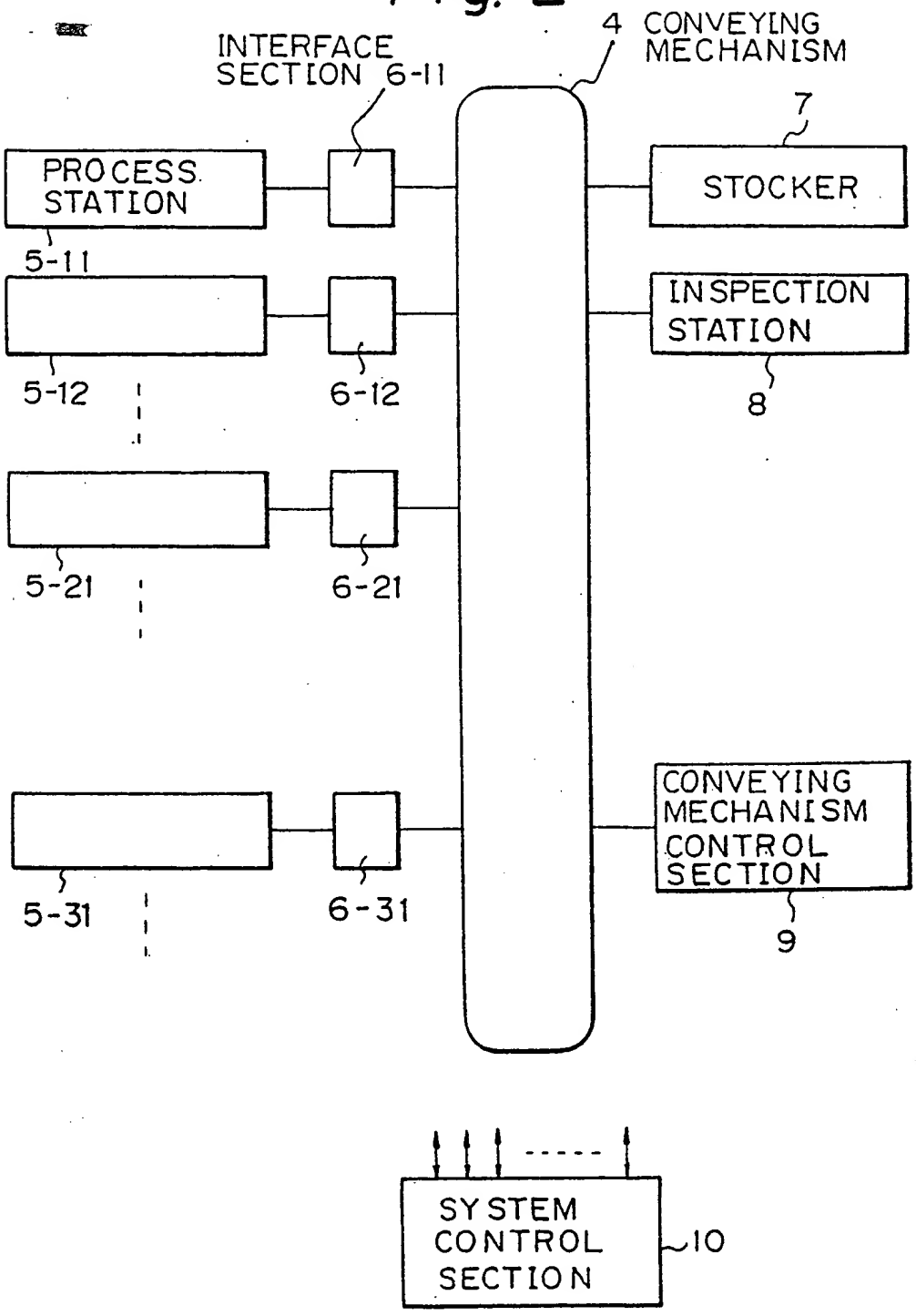

INTERFACE SECTION 6-11
4 CONVEYING MECHANISM
7
PROCESS STATION
STOCKER
5-11
INSPECTION STATION
5-12
6-12
8
5-21
6-21
CONVEYING MECHANISM CONTROL SECTION
5-31
6-31
9
SYSTEM CONTROL SECTION
10

Fig. 3

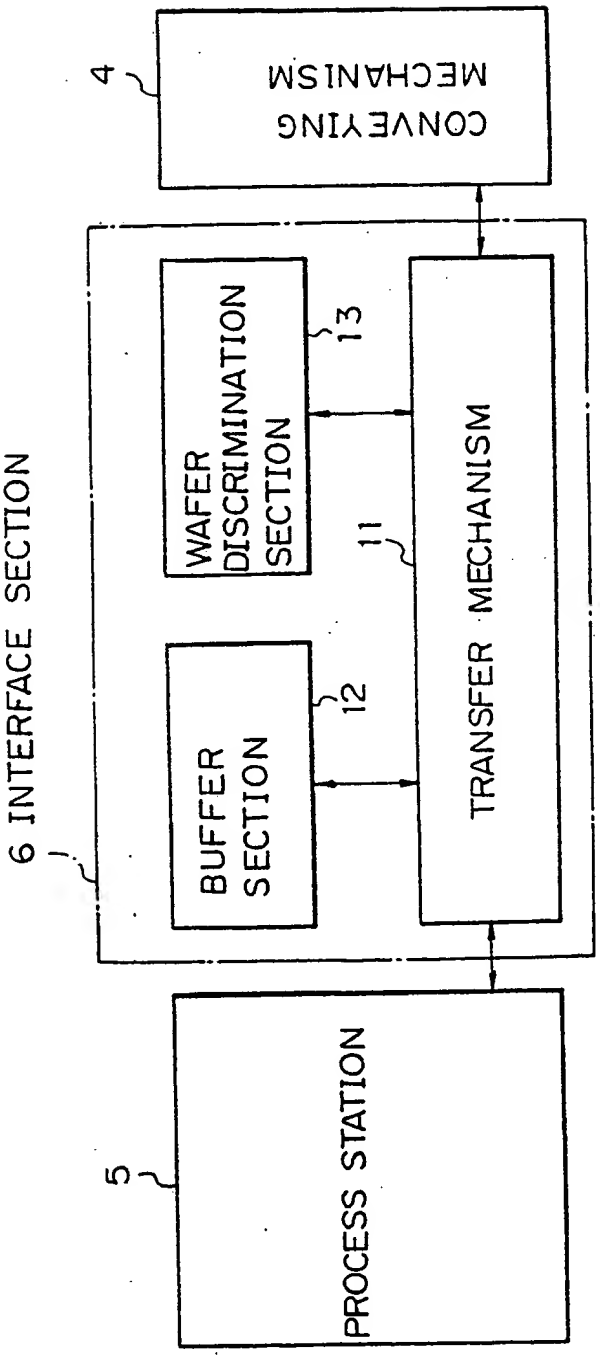

4
CONVEYING MECHANISM
6 INTERFACE SECTION
WAFER DISCRIMINATION SECTION
13
11
BUFFER SECTION
12
TRANSFER MECHANISM
5
PROCESS STATION

Fig. 4

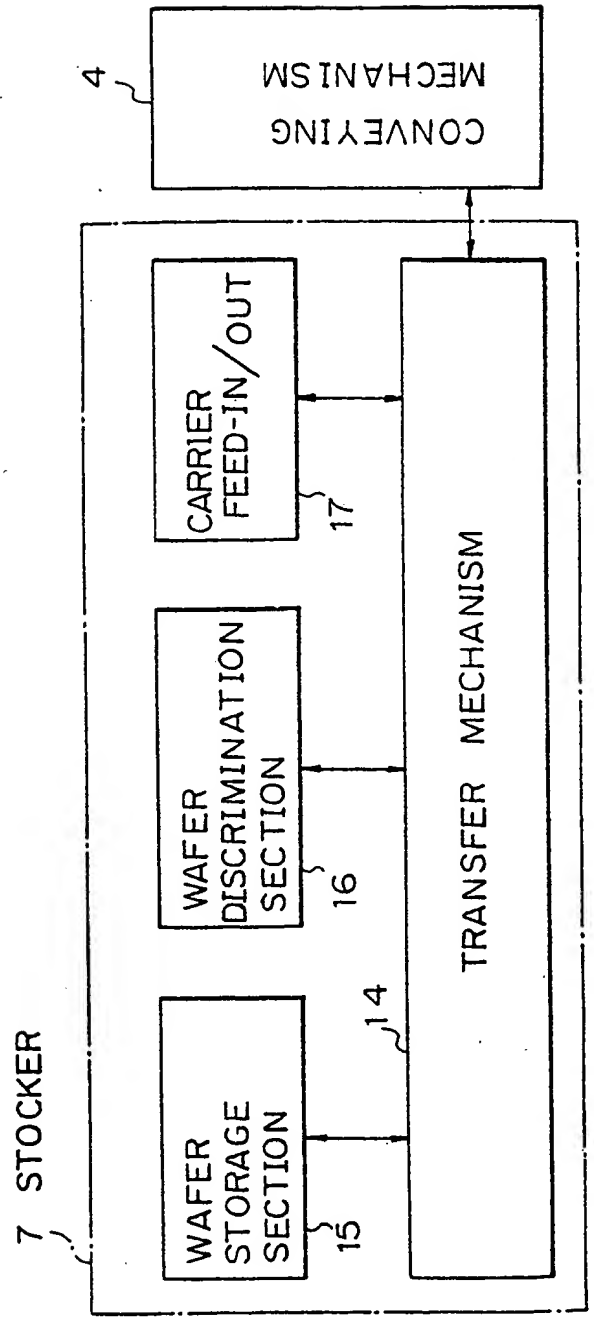

4
CONVEYING MECHANISM
7 STOCKER
WAFER STORAGE SECTION
15
WAFER DISCRIMINATION SECTION
16
CARRIER FEED-IN/OUT
17
14
TRANSFER MECHANISM

Fig. 5A

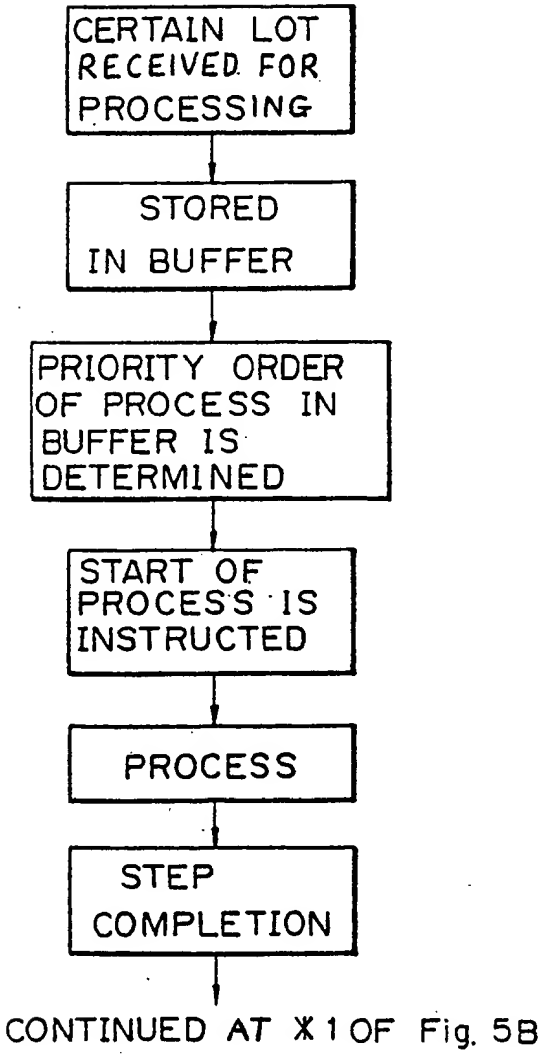
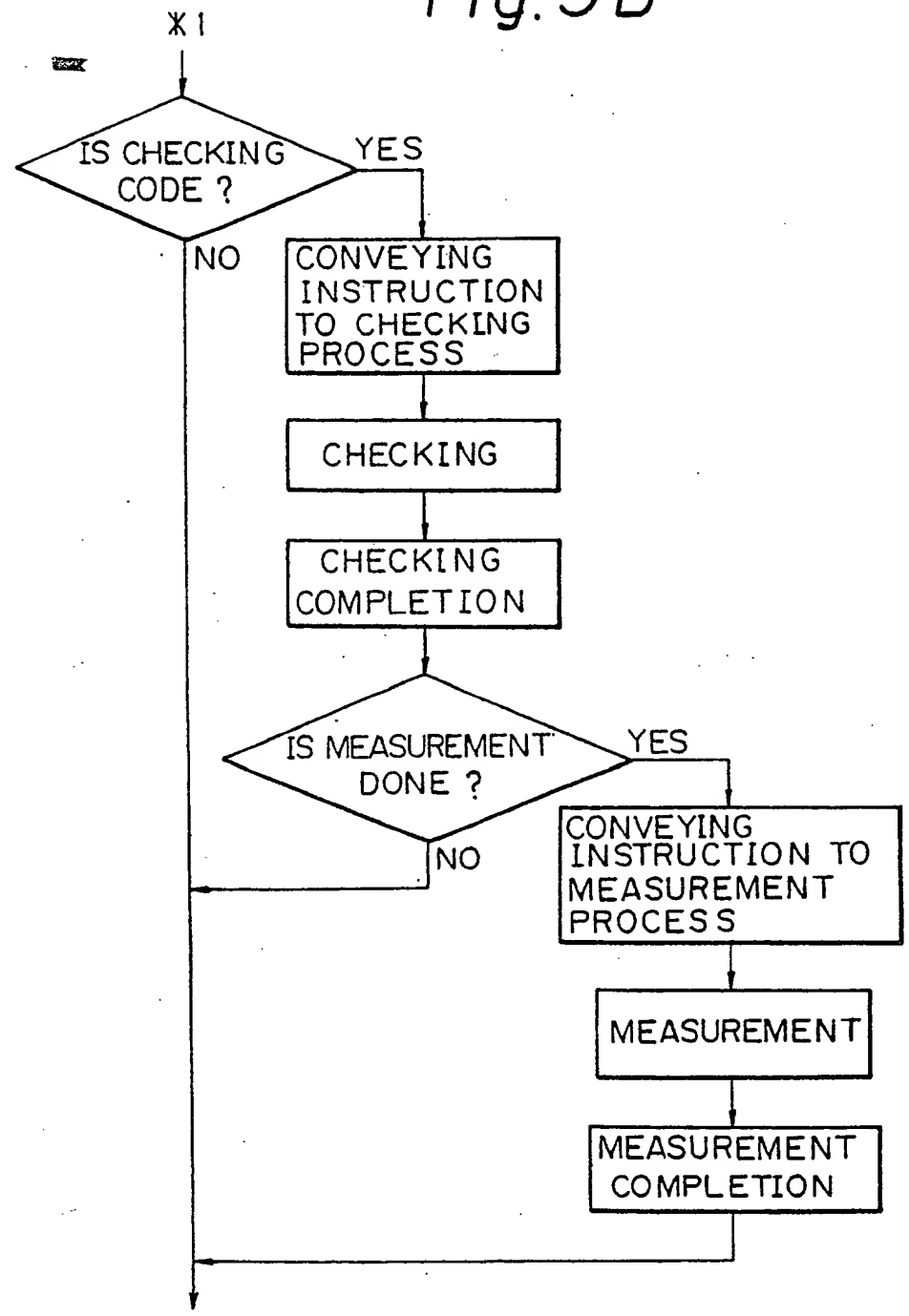

CERTAIN LOT RECEIVED FOR PROCESSING
STORED IN BUFFER
PRIORITY ORDER OF PROCESS IN BUFFER IS DETERMINED
START OF PROCESS IS INSTRUCTED
PROCESS
STEP COMPLETION
CONTINUED AT X1 OF Fig. 5B

Fig. 5B



CONTINUED AT ※2 OF Fig. 5C

Fig. 5C

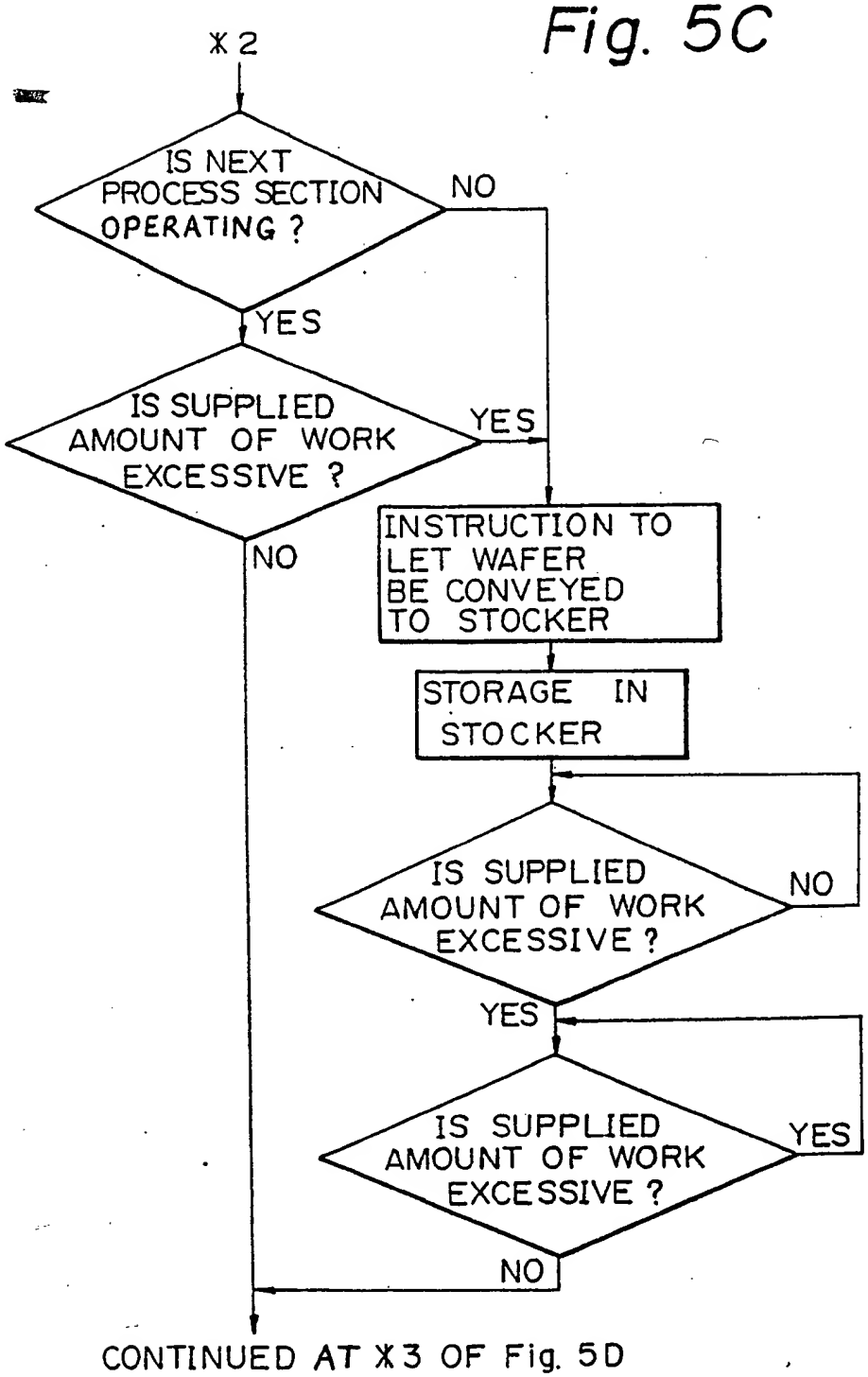

X2
IS NEXT PROCESS SECTION OPERATING ?
NO
YES
IS SUPPLIED AMOUNT OF WORK EXCESSIVE ?
YES
NO
INSTRUCTION TO LET WAFER BE CONVEYED TO STOCKER
STORAGE IN STOCKER
IS SUPPLIED AMOUNT OF WORK EXCESSIVE ?
NO
YES
IS SUPPLIED AMOUNT OF WORK EXCESSIVE ?
YES
NO
CONTINUED AT X3 OF Fig. 5D

Fig. 5D

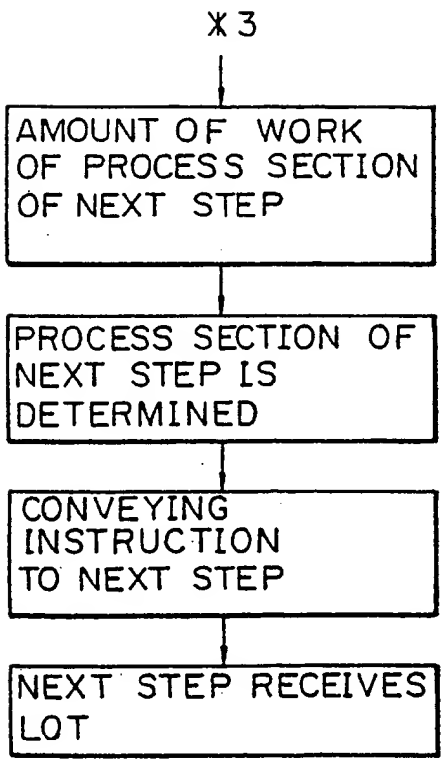

X3
AMOUNT OF WORK OF PROCESS SECTION OF NEXT STEP
PROCESS SECTION OF NEXT STEP IS DETERMINED
CONVEYING INSTRUCTION TO NEXT STEP
NEXT STEP RECEIVES LOT

Fig. 6A

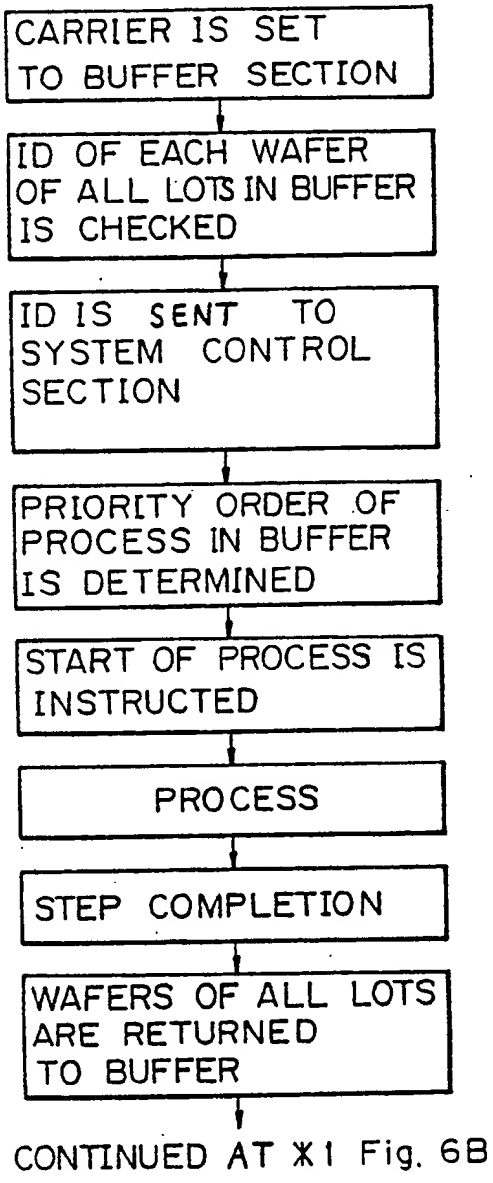

CARRIER IS SET TO BUFFER SECTION
ID OF EACH WAFER OF ALL LOTS IN BUFFER IS CHECKED
ID IS SENT TO SYSTEM CONTROL SECTION
PRIORITY ORDER OF PROCESS IN BUFFER IS DETERMINED
START OF PROCESS IS INSTRUCTED
PROCESS
STEP COMPLETION
WAFERS OF ALL LOTS ARE RETURNED TO BUFFER
CONTINUED AT X1 Fig. 6B

Fig. 6 B

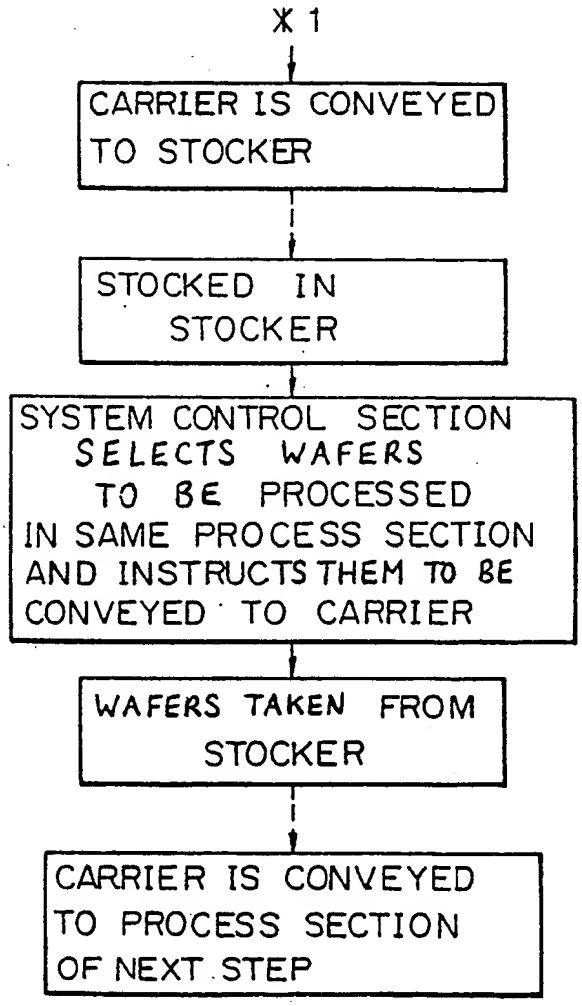

X 1
CARRIER IS CONVEYED TO STOCKER
STOCKED IN STOCKER
SYSTEM CONTROL SECTION SELECTS WAFERS TO BE PROCESSED IN SAME PROCESS SECTION AND INSTRUCTS THEM TO BE CONVEYED TO CARRIER
WAFERS TAKEN FROM STOCKER
CARRIER IS CONVEYED TO PROCESS SECTION OF NEXT STEP

Fig. 7

Fig. 7A
Fig. 7B

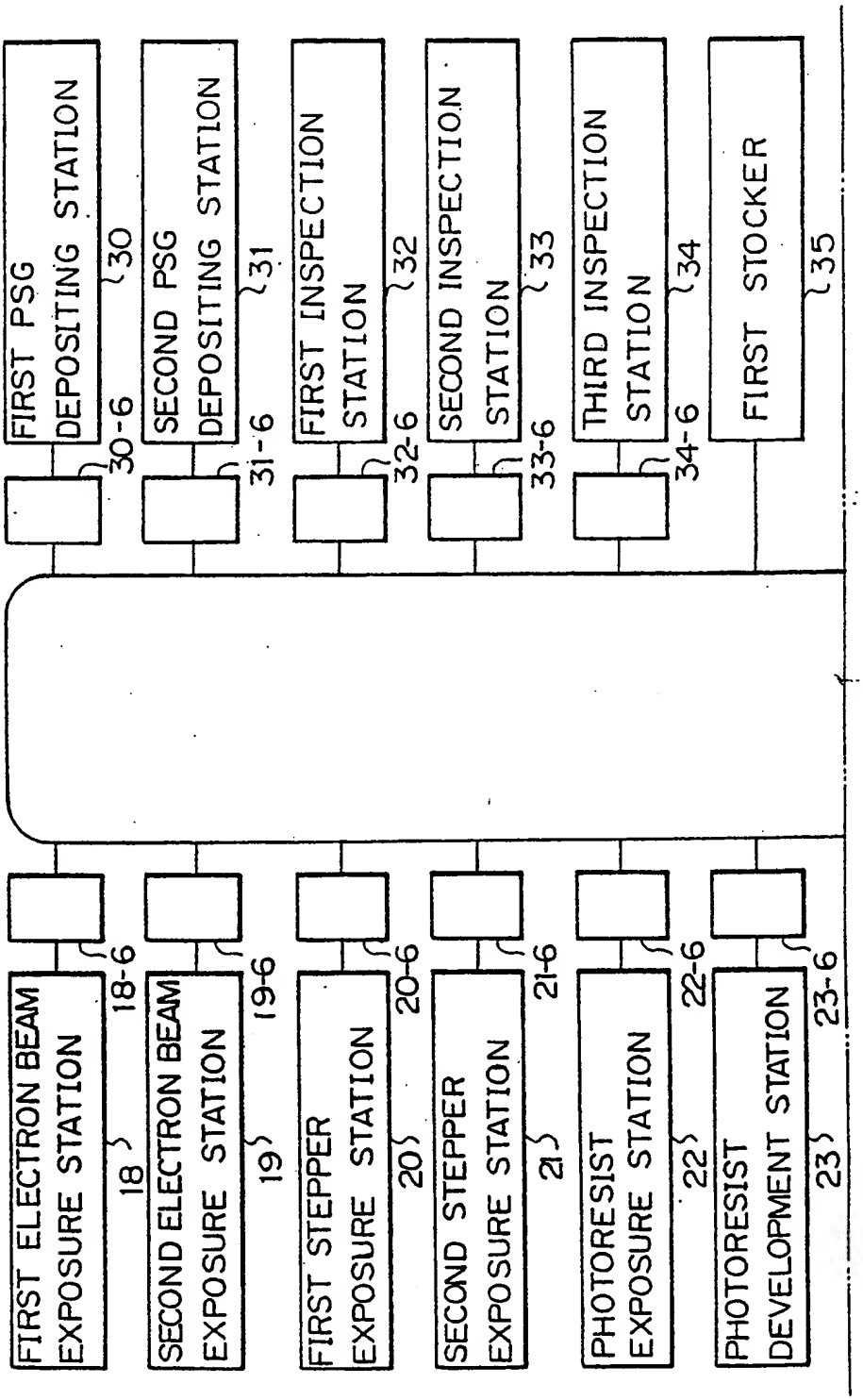


Fig. 7A

Fig. 7B

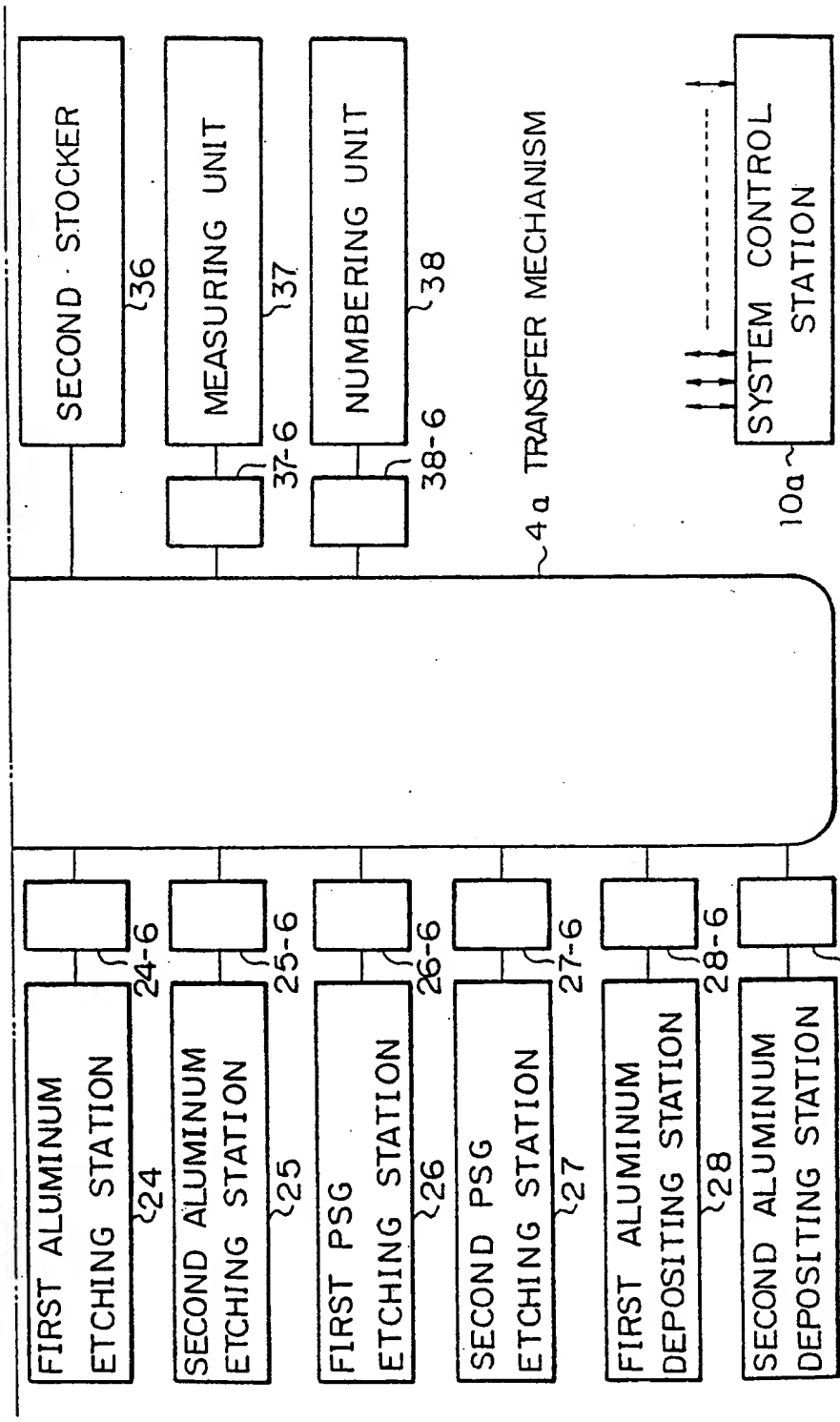

SECOND STOCKER
36
MEASURING UNIT
37
37-6
NUMBERING UNIT
38
38-6
4a TRANSFER MECHANISM
SYSTEM CONTROL STATION
10a
FIRST ALUMINUM ETCHING STATION
24
24-6
SECOND ALUMINUM ETCHING STATION
25
25-6
FIRST PSG ETCHING STATION
26
26-6
SECOND PSG ETCHING STATION
27
27-6
FIRST ALUMINUM DEPOSITING STATION
28
28-6
SECOND ALUMINUM DEPOSITING STATION
29
29-6

Fig. 8

Fig. 8A

Fig. 8B

Fig. 8A

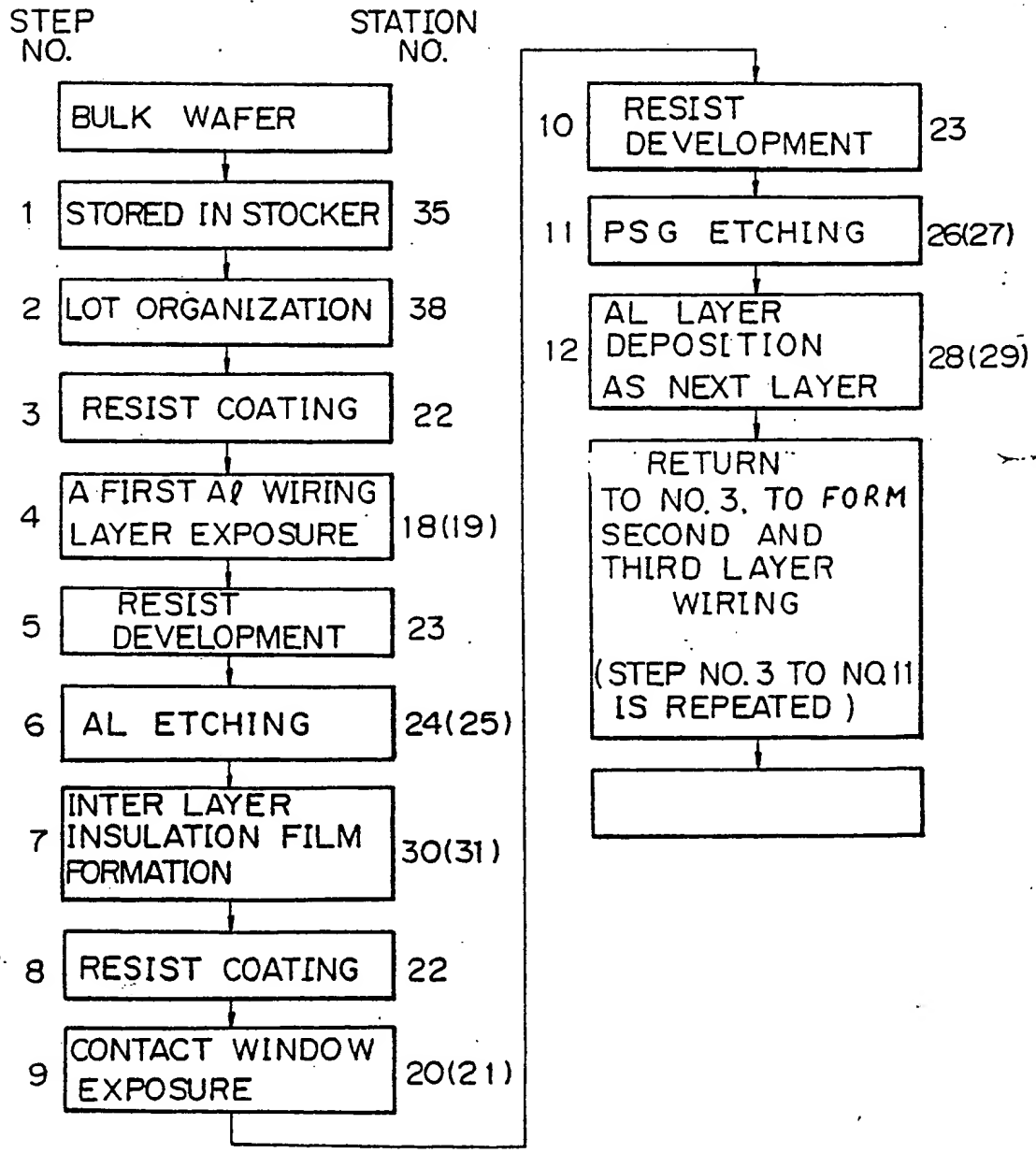


Fig. 8 B

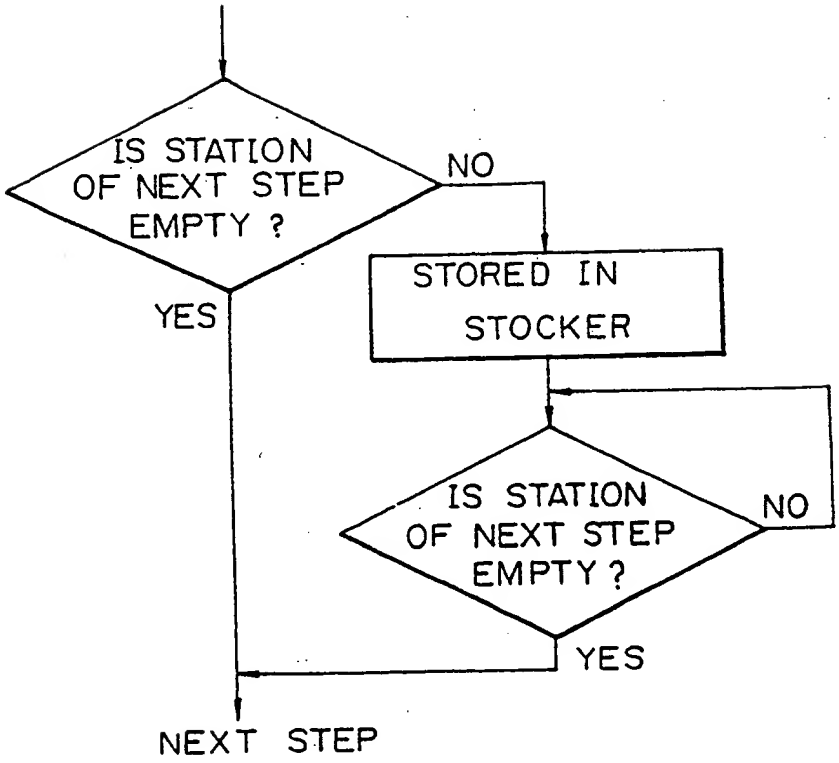

IS STATION OF NEXT STEP EMPTY ?
NO
YES
STORED IN STOCKER
IS STATION OF NEXT STEP EMPTY ?
NO
YES
NEXT STEP

Fig. 9

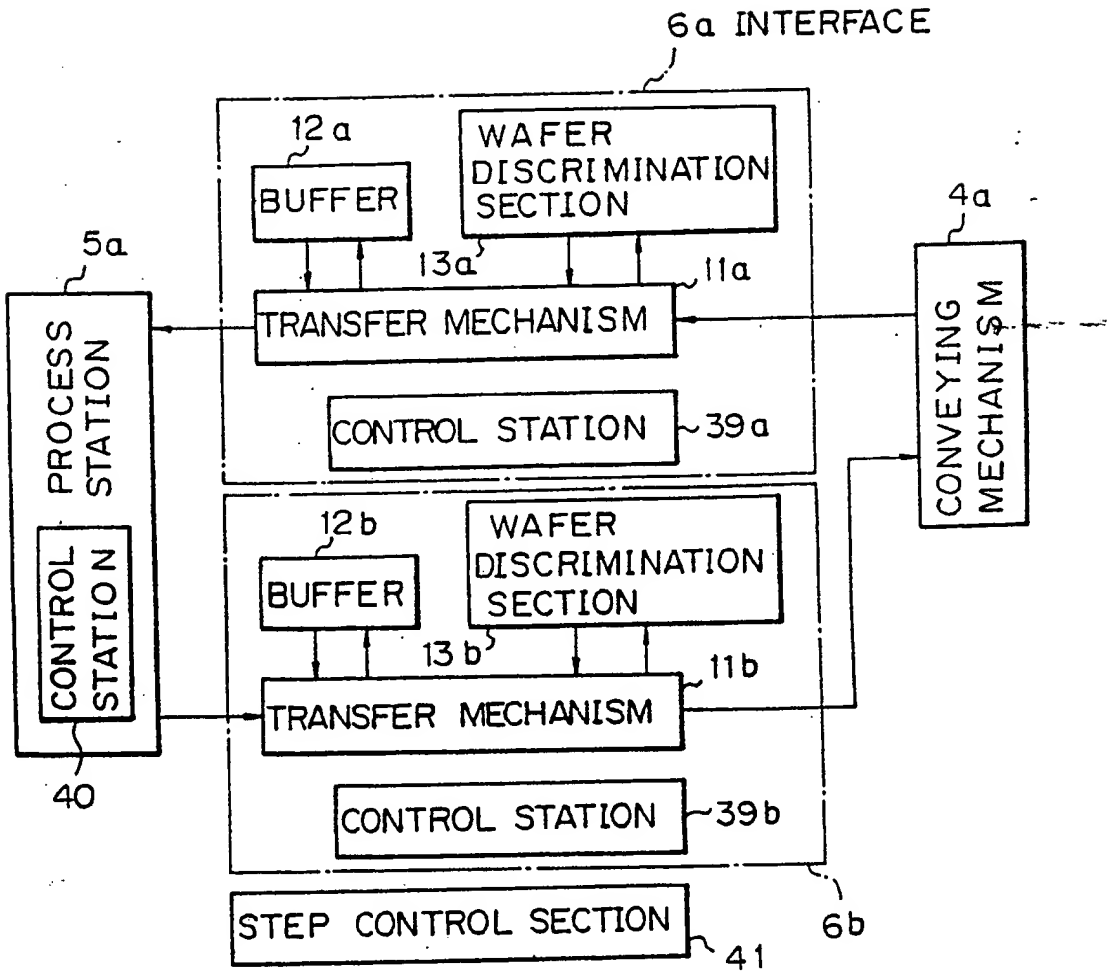
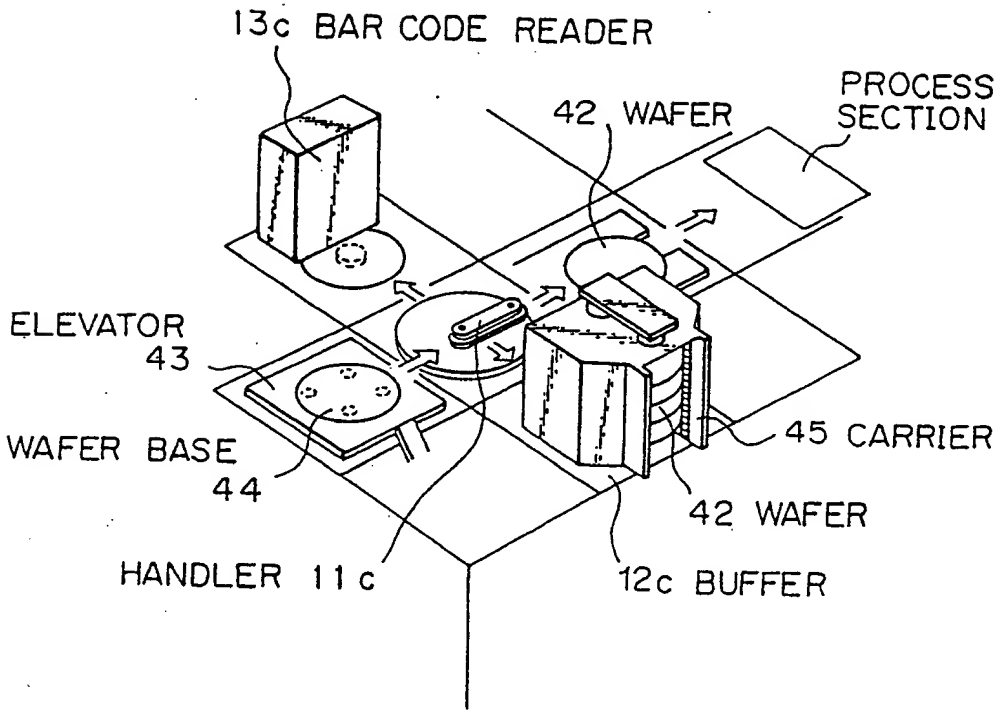
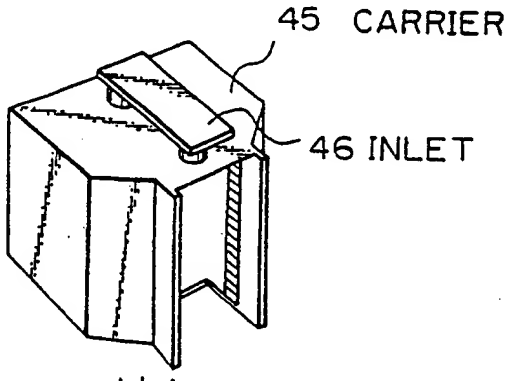

6a INTERFACE
12a
BUFFER
WAFER DISCRIMINATION SECTION
4a
5a
13a
11a
PROCESS STATION
TRANSFER MECHANISM
CONVEYING MECHANISM
CONTROL STATION
39a
12b
WAFER DISCRIMINATION SECTION
BUFFER
CONTROL STATION
13b
11b
TRANSFER MECHANISM
40
CONTROL STATION
39b
STEP CONTROL SECTION
41
6b

Fig. 10


13c BAR CODE READER
42 WAFER
PROCESS SECTION
ELEVATOR 43
WAFER BASE 44
45 CARRIER
42 WAFER
HANDLER 11c
12c BUFFER

(a)


45 CARRIER
46 INLET

(b)

Fig. 11

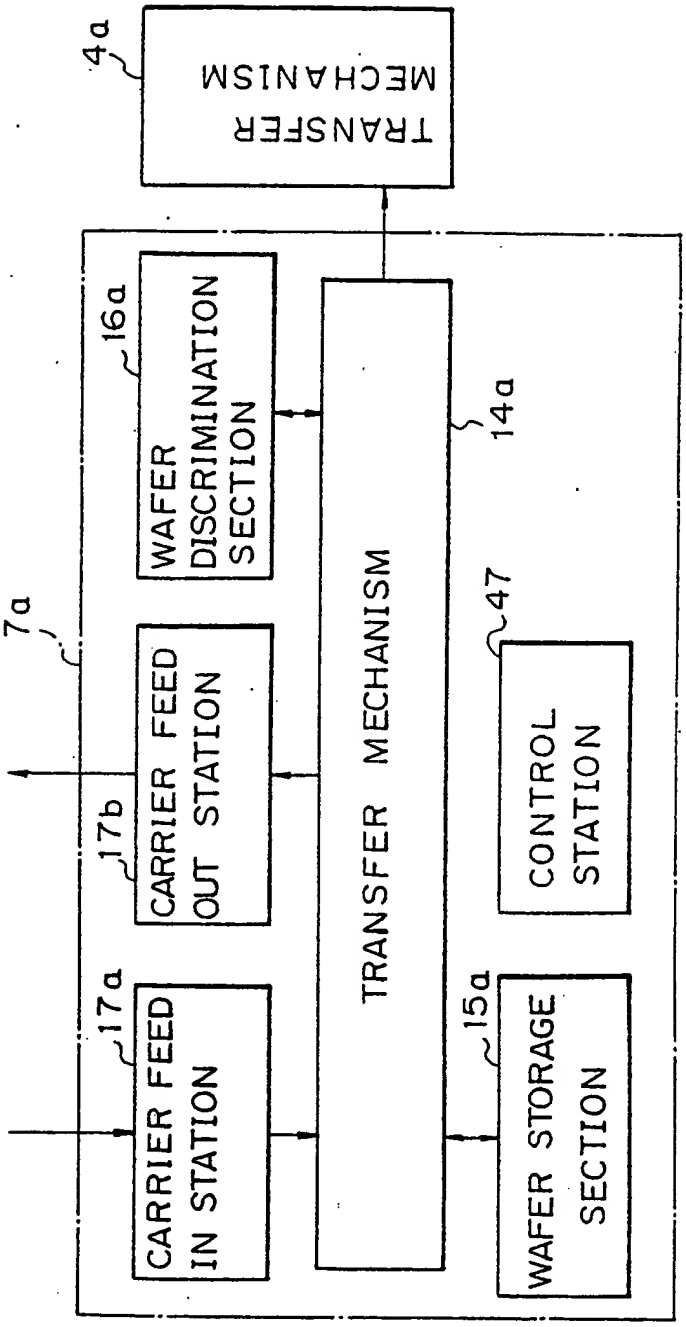

4a
TRANSFER MECHANISM
16a
WAFER DISCRIMINATION SECTION
14a
7a
17b
CARRIER FEED OUT STATION
TRANSFER MECHANISM
47
CONTROL STATION
17a
CARRIER FEED IN STATION
15a
WAFER STORAGE SECTION

Fig. 12

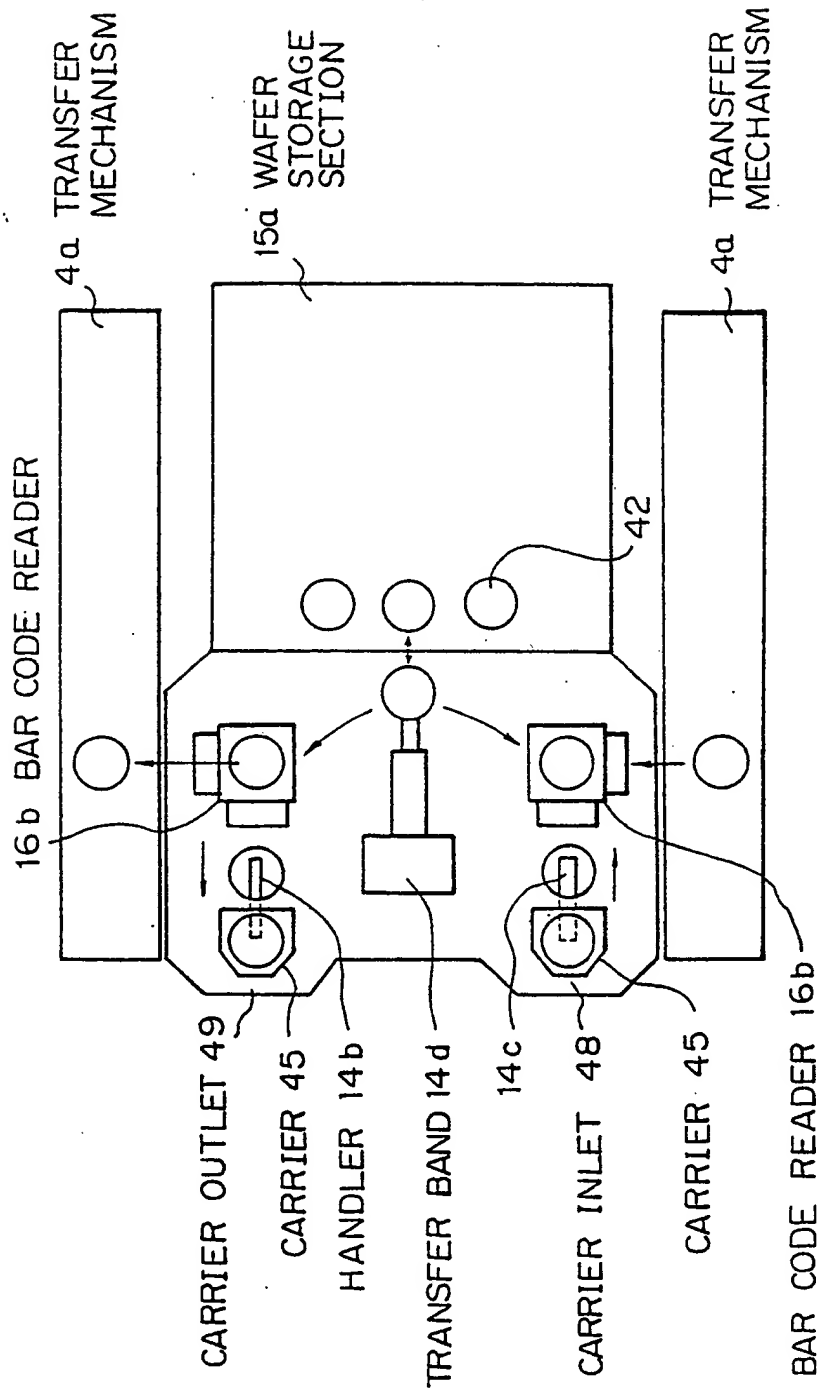

4a TRANSFER MECHANISM
15a WAFER STORAGE SECTION
4a TRANSFER MECHANISM
16b BAR CODE READER
42
CARRIER OUTLET 49
CARRIER 45
HANDLER 14b
TRANSFER BAND 14d
14c
CARRIER INLET 48
CARRIER 45
BAR CODE READER 16b

Fig. 13

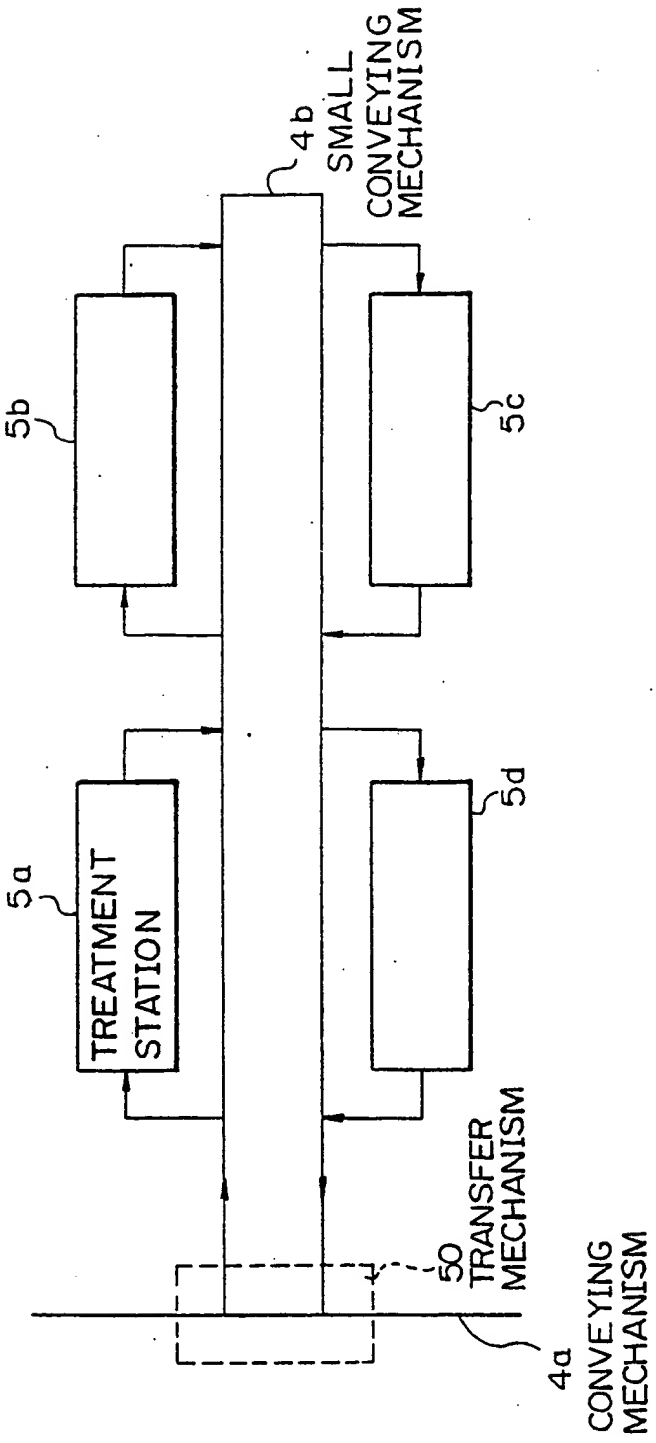
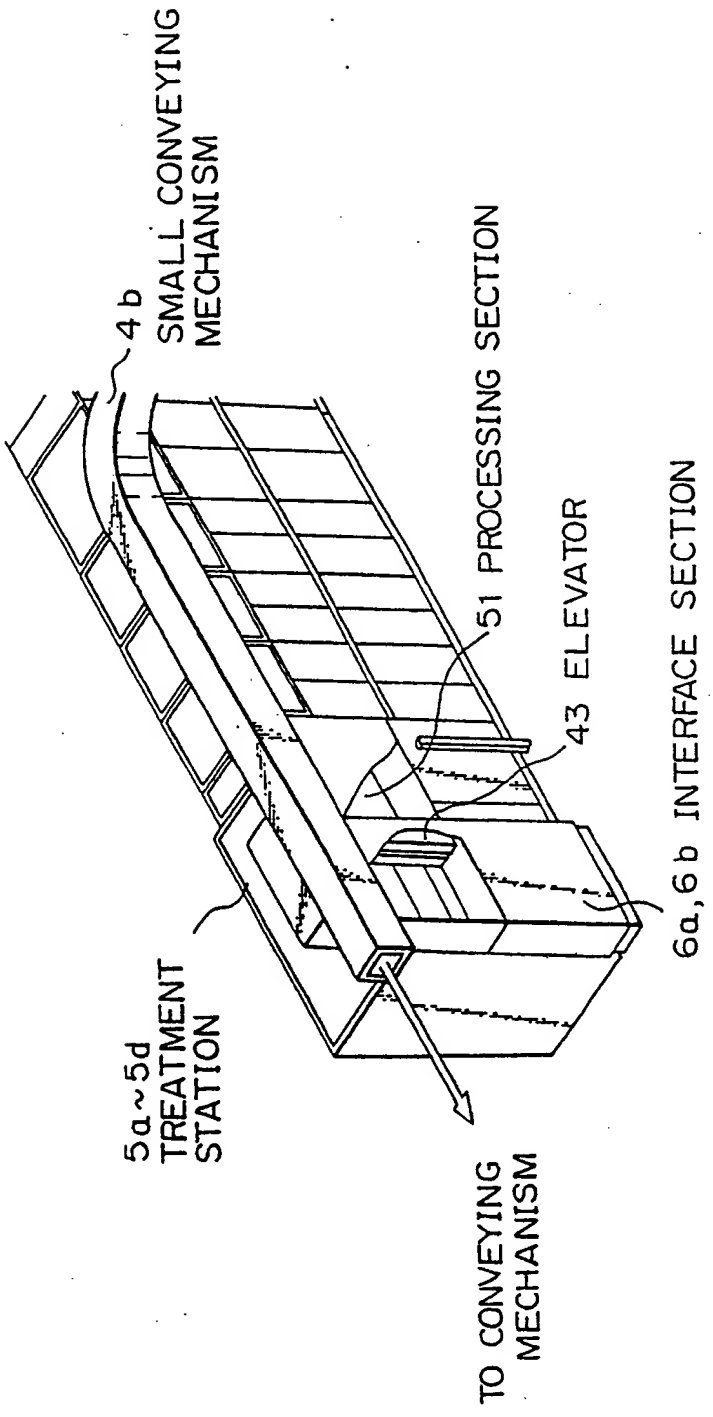

4b
SMALL
CONVEYING
MECHANISM
5b
5c
5a
TREATMENT
STATION
5d
50
TRANSFER
MECHANISM
4a
CONVEYING
MECHANISM

Fig. 14


4 b
SMALL CONVEYING MECHANISM
51 PROCESSING SECTION
43 ELEVATOR
6a, 6 b INTERFACE SECTION
5a~5d TREATMENT STATION
TO CONVEYING MECHANISM

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(71) Applicant: FUJITSU LIMITED
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211(JP)

(72) Inventor: Kiriseko, Tadashi
3-6-16, Wakabadai Shiroyama-cho
Tsukui-gun Kanagawa 220-01(JP)

Inventor: Tani, Hiromichi
109, 2-79-18, Furuichiba Saiwai-ku
Kawasaki-shi Kanagawa 211(JP)
Inventor: Soma, Noriko
1-6-5-405, Utsukushigaoka Midori-ku
Yokohama-shi Kanagawa 277(JP)
Inventor: Shigemi, Nobuhisa
Rm. 307, Dai-8 Nakahara-ryo, 1674,
Shimokodanaka
Nakahara-ku Kawasaki-shi Kanagawa 211(JP)
Inventor: Toyoda, Takayuki
28, Uchihori-cho Yokkaichi-shi
Mie 510(JP)

(74) Representative: Stebbing, Timothy Charles et al
Haseltine Lake & Co. Hazlitt House 28
Southampton Buildings Chancery Lane
London WC2A 1AT(GB)

(54) Continuous semiconductor substrate processing system.

(57) A continuous semiconductor substrate processing system comprising a plurality of different process stations (5-11,5-12,...) for performing respective predetermined processes on semiconductor wafers and a semiconductor wafer conveying mechanism (4) coupled to the individual semiconductor wafer process stations. Each process station is coupled to the conveying mechanism via an interface section (6-11,6-12,...) including a transfer mechanism (11) for transferring semiconductor wafers between the conveying mechanism (4) and each process station (5-11,5-12,...), a discrimination section (13) for discriminating the semiconductor wafers, and a buffer section (12) for temporarily storing the semiconductor wafers. The continuous semiconductor wafer processing system further comprises: a stocker (7) coupled to the conveying mechanism (4) for temporarily accommodating semiconductor wafers during processing and including a storage section (15) for storing semiconductor wafers, a transfer mechanism (14) for transferring semiconductor wafers between said storage section and said conveying mechanism (4), a discrimination section (16) for discriminating semiconductor wafers, and a carrier feed-in feed-out section (17) capable of feeding in and feeding out semiconductor wafers; a conveying mechanism; and a system control section (10) for communicating with and controlling the process stations (5-11,5-12,...), interface sections (6-11,6-12,...), stocker (7) and conveying mechanism control section (9).

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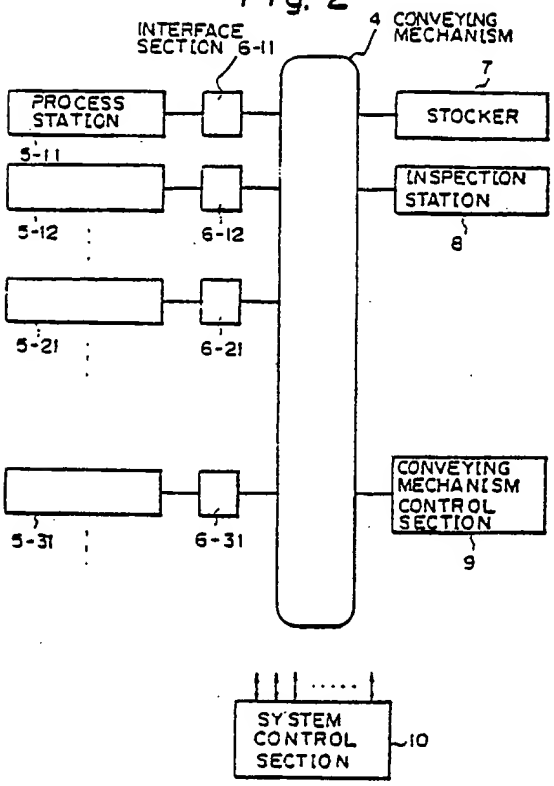
Fig. 2


INTERFACE SECTION 6-11
4 CONVEYING MECHANISM
7
PROCESS STATION
5-11
STOCKER
INSPECTION STATION
8
5-12
6-12
5-21
6-21
CONVEYING MECHANISM CONTROL SECTION
9
5-31
6-31
SYSTEM CONTROL SECTION
10

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 30 9250

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	GB-A-2056169 (SUZUKI)		H01L21/00
A	WO-A-8703979 (ASYST TECHNOLOGIES)		
A	US-A-4717681 (CURRAN)		
A	US-A-3946484 (INTERNATIONAL BUSINESS MACHINES)		

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	06 NOVEMBER 1990	BERTIN M.H.J.

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